JAPANESE JOURNAL OF APPLIED PHYSICS
VOL. 29, NO. 2, FEBRUARY, 1990, pp. L 195–L 197

Dependence of the Carrier Concentration Profile at the Si MBE Layer/p-Si Substrate Interface on the Si Substrate Preparation Method

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(Received November 10, 1989; accepted for publication January 11, 1990)

The influence of the Si substrate preparation method on the carrier concentration profile at the Si MBE layer/p-Si substrate interface was studied. It was found that the Si substrate should be placed in the UHV MBE chamber immediately (within 10 minutes) after removal of the oxide layer to eliminate the p^+ interface layer and must be heated up to 1250°C before MBE growth, in order to prevent carrier depletion at the interface and also to obtain good I–V characteristics of a diode with a Silicide/p-Si (or SiGe) MBE layer/p-Si substrate structure.

KEYWORDS: Si, SiGe, molecular beam epitaxy, oxide layer, carrier concentration profile, interface, Schottky diode

§1. Introduction

A PtSi/p-Si Schottky contact is now used for a large-scale IR image sensor in the wavelength range of 3 ~ 5 μm.[1] Since the absorption of infrared (IR) radiation in the atmosphere is very small in the wavelength range of 8 ~ 12 μm, and the radiation peak of the object at room temperature is around 10 μm, an IR image sensor for this long-wavelength range is very important. Therefore, further extension of the cutoff wavelength is urgently needed especially in the weather satellite field.[2]

We have been studying Pt/p-$Si_{1-x}Ge_x$/p-Si Schottky contacts aiming at a longer wavelength IR sensor and have demonstrated that the Schottky barrier heights can be reduced by increasing the Ge fraction.[3] One of the obstacles to realization of a Pt/p-$Si_{1-x}Ge_x$ IR sensor is a low breakdown voltage of the Pt/p-$Si_{1-x}Ge_x$ Schottky diodes. In order to realize a guard ring structure for the 10 μm-range CCD image sensor in the future and to utilize a strained SiGe layer,[4] the epitaxial layer should be as thin as possible. It was reported, however, that a p-type high carrier concentration ($10^{17} \sim 10^{18}$ cm^{-3}) region often appears at the interface between the Si MBE layer and p-type Si substrate.[5,6] This high carrier concentration layer must influence the breakdown voltage of the Pt/p-$Si_{1-x}Ge_x$/p-Si substrate Schottky diodes when the epitaxial layer is thin.

Kubiak *et al.* reported that this heavily p-type layer at the interface was formed by Boron introduced from the borosilicate glass of the viewport in the MBE system.[5] On the other hand, Casel *et al.* demonstrated a strong dependence of the interface p^+ layer on the existence of the surface oxide layer of the Si substrate.[6] It is widely accepted that a carefully prepared surface oxide layer is inevitable to obtain a high quality Si MBE layer.[7] It is not yet known how to compromise these two conflicting phenomena; the oxide layer is necessary for a high quality MBE layer, but it introduces a Boron-doped p^+ layer at the interface.

The purpose of this work is to find a preparation and cleaning method for the Si substrate to obtain a high quality Si and SiGe MBE layer without the p^+ interface region at the epi-substrate interface.

§2. Experimental

MBE layers were grown on p-type (100) Czochralski Si substrates ($p = 3 \sim 5 \times 10^{16}$ cm^{-3}). The base pressure of the MBE system was about 3×10^{-10} Torr and that of the load lock chamber was about 10^{-7} Torr. Si was evaporated by an E-gun and Ge, by a K-cell. The Si and Ge molecular beams were controlled by monitoring with an electron impact emission spectroscopy (EIES) sensor. Si layers were grown at 750°C at a rate of 1.5 Å/s. SiGe layers were grown at 550°C at a rate of 1.5 ~ 2.0 Å/s. The pressure during the growth was $1 \sim 3 \times 10^{-9}$ Torr. The Boron was doped in both layers with HBO_2. The substrate cut in 2 cm squares was precleaned by the usual Ishizaka-Shiraki method.[7] For some substrates, the passivation oxide layers were completely removed by a diluted HF (0.5%) solution before the substrates were placed in the MBE chamber. The substrate in the MBE chamber was heated up to about 850°C to evaporate the surface oxide layer before the Si growth. In some cases, the substrate was heated up to 1250°C to remove the Carbon on the substrate. Carrier concentration profiles at the interface were calculated from the capacitance-voltage (C–V) characteristics measured by a Ti Schottky contact.

§3. Results and Discussion

Because Kubiak *et al.* reported that the accumulation of Boron at the Si epi-substrate interface was related to the thickness of the passivation oxide layer, we first investigated dependence of the Boron accumulation on the thickness of the oxide layer. After formation of the passivation oxide layer by Ishizaka-Shiraki method, the

oxide layer was thinned by a diluted HF solution (0.5%), and Si substrates with three different oxide layers (0, ~5, ~15 Å) were formed.

Figure 1 shows the carrier concentration profiles at the MBE Si layer/p-Si substrate interfaces. Arrows in the figure indicate positions of the MBE Si layer/p-Si sub interfaces. The thickness of the oxide layer of sample A was zero, that of sample B was about 5 Å and that of sample C (whose oxide layer was not removed by the diluted HF solution) was about 15 Å. The thickness of the oxide layer was estimated by the etching rate of the oxide layer. Sample A was placed in the UHV MBE chamber within 10 minutes after removal of the oxide layer, without rinsing in water to avoid oxidation of the substrate surface by the water. Samples B and C were rinsed in water after etching by the diluted HF. These samples were heated to evaporate the oxide layers. Sample A showed a 2×1 RHEED pattern at 400°C, sample B showed it at 680°C and sample C showed it at 850°C. No SiC RHEED pattern was observed for these samples. Samples B and C show almost the same height of the carrier concentration peak in Fig. 1, but sample A does not. These results indicate that the p^+-layer at the interface can be reduced by removing the oxide layer as reported by Casel *et al.*[6] It is not well known where the Boron comes from. It might be from borosilicate glass,[5] but other candidates are the substrate and atmosphere itself. In any case, when the oxide layer exists, the Boron is thought to accumulate in the oxide layer from the surroundings and to be left on the substrate surface when the oxide layer is evaporated.

When the oxide passivation film was thinned by the diluted HF, the SiC RHEED pattern was often observed on the surface when the Si substrate was heated up to above 750°C. Figure 2 shows the carrier concentration profile at the Si MBE layer/p-Si substrate interfaces of

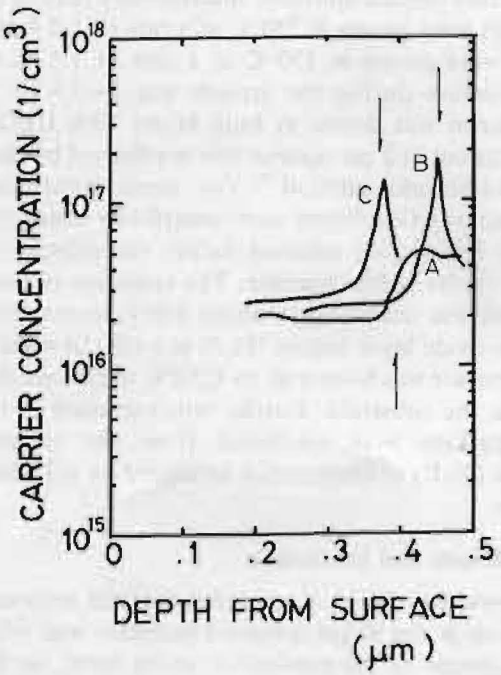

Fig. 1. Carrier concentration profiles at the Si MBE layer/p-Si substrate interfaces. The thicknesses of oxide layers were as follows: sample A was zero, B was 5 Å and C was 15 Å.

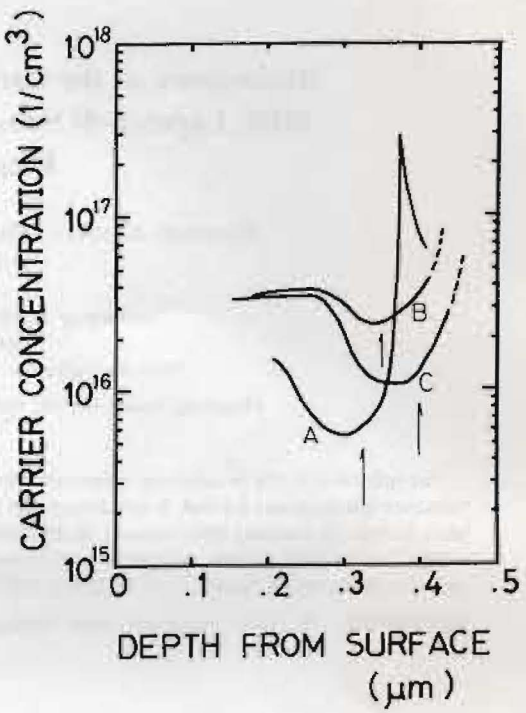

Fig. 2. Carrier concentration profiles at the Si MBE layer/p-Si sub interface. The thicknesses of oxide layers were as follows: sample A was zero, B and C were 5 Å. All of them were kept in the load-lock chamber for 2 hours.

the samples on which the SiC RHEED patterns were observed. The thickness of the oxide layer of sample A in Fig. 2 was zero: those of B and C were about 5 Å. All of them were kept in the load-lock chamber (10^{-7} Torr) for 2 hours before being heated up to 850°C in the UHV MBE chamber to evaporate the oxide layer. The intensities of the SiC RHEED patterns of samples A and C were stronger than that of sample B. Depletion regions of the carrier appeared at the MBE layer-substrate interfaces for all samples. The cause of the depletion region was thought to be some defects in the MBE grown layer which were introduced by SiC on the substrate surface. For sample A, a 2×1 RHEED pattern was not observed until the substrate temperature of 650°C, although the oxide layer was completely removed. This is probably due to formation of the oxide layer of a few Å while the sample was kept in the load-lock chamber for 2 hours. Thus both a depletion and a high carrier concentration region appeared in sample A. In spite of the oxide layer existing in samples B and C, the high carrier concentration region did not appear. This is probably due to the fact that the diode breakdown occurrs before the depletion layer reaches to the high carrier concentration region.

To clarify the origin of the depletion layer, Si substrates were heated up to 1250°C to evaporate Carbon on the substrate surface. Samples A and B shown in Fig. 3 were kept in the load-lock chamber for 2 hours after complete removal of the oxide layer by a diluted HF solution. Sample A was heated up to 850°C, sample B was heated up to 1250°C and held there for 10 minutes. Sample C was placed in the UHV MBE chamber within 10 minutes after removal of the oxide layer, heated up to

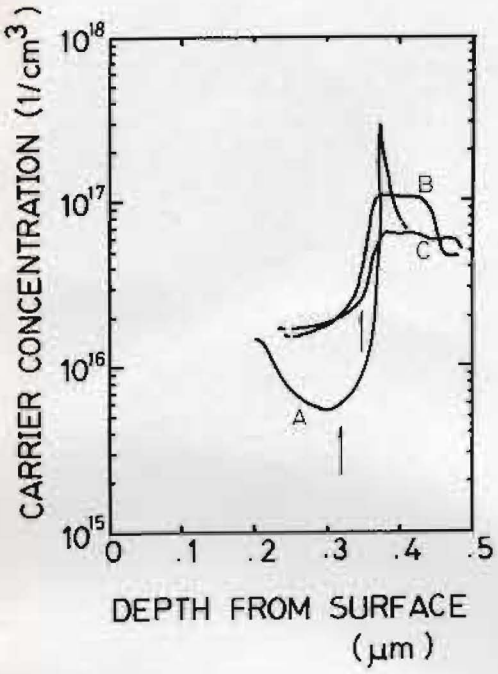

Fig. 3. Carrier concentration profiles at the Si MBE layer/p-Si substrate interfaces. The thicknesses of oxide layers were zero in all samples. Sample A was heated up to 850°C: B and C were heated up to 1250°C. Samples A and B were kept in the load-lock chamber for 2 hours, and sample C was placed in the UHV MBE chamber within 10 minutes.

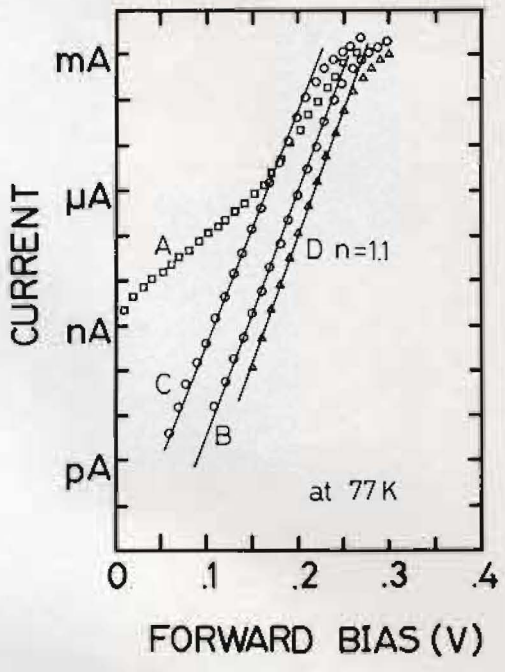

Fig. 4. Forward I–V characteristics of Pd/MBElayer/p-Si substrate Schottky diodes. Structures of the MBE layers are as follows: samples A and B are p-Si(3000 Å)/p-Si sub, sample C is p-$Si_{0.9}Ge_{0.1}$(2000 Å)/p-Si sub, sample D is p-Si substrate only. Sample A was heated up to 850°C, and samples B and C were heated up to 1250°C.

1250°C and held there for 10 minutes. The depletion region disappeared for sample B probably due to elimination of Carbon on the substrate surface, but a high carrier concentration region still existed though it was broadened by the 1250°C thermal treatment. On the other hand, sample C had neither a depletion layer nor a high carrier concentration region, similar to curve A in Fig. 1. This was probably because there was no oxide layer and no SiC on the substrate surface due to the 1250°C thermal treatment. These results indicate that the oxide layer formed in the load-lock chamber also makes a high carrier concentration region, and only when there is no oxide layer and no SiC on the substrate does, neither the depletion region nor the high carrier concentration region appear at the interface.

Influence of the heat treatment at 1250°C on the I–V characteristics was investigated as the next step. Figure 4 shows comparison of the I–V characteristics of Pd Schottky diodes at 77 K for the samples heated up to 1250°C and up to only 850°C. The structures of samples A ~ D in Fig. 4 were as follows: samples A and B were p-Si(3000 Å)/p-Si substrate, sample C was p-$Si_{0.9}Ge_{0.1}$(2000 Å)/p-Si substrate and sample D was p-Si substrate only. As for the heat treatment, sample A was heated up to 850°C for 10 minutes before the growth, and samples B and C were heated up to 1250°C for 10 minutes. Sample A, which was heated up to only 850°C, had a large leak current, but the others did not. These results indicate that in order to get good I–V characteristics, it is necessary to place the substrate in the UHV MBE chamber immediately after removal of the oxide layer and heat it up to 1250°C before MBE growth to eliminate the Carbon on the substrate surface. In practical device processes, however, other low-temperature process, such as O^+ beam irradiation to remove the Carbon on the surface, must be developed to reduce the thermal damage to processed wafers.

Acknowledgement

The authors would like to thank Miss. Y. Cho and Mr. M. Nishitsuji for their help with C–V and I–V measurements. This work was partly supported by a Grant in Aid for Scientific Research from the Ministry of Education, Science and Culture of Japan.

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